

## CLAIMS

1 1. A verification system controlled by a master clock for verifying the proper operation of a  
2 user circuit design, comprising:  
3 reception logic for receiving input data to be evaluated within an evaluation time;  
4 evaluation logic for modeling the user circuit design in reconfigurable hardware logic and  
5 evaluating the input data during the evaluation time; and  
6 clock generation logic for generating a plurality of asynchronous clocks for use by the  
7 evaluation logic and controlling the phase relationship among the plurality of asynchronous  
8 clocks.

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1 2. The system of claim 1, wherein the reconfigurable hardware logic in the evaluation logic  
includes at least one reconfigurable hardware logic chip.

1 3. The system of claim 2, wherein the reconfigurable hardware logic chip includes at least  
one field programmable gate array (FPGA) chip.

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1 4. The system of claim 3, wherein the clock generation logic includes:  
2 a plurality of clock generation slices for generating a plurality of clocks, where each clock  
3 generation slice generates a clock in response to a trigger signal; and  
4 a clock scheduler for generating the trigger signal to the plurality of clock generation  
5 slices so that the generation of the clocks by the plurality of clock generation slices is scheduled in  
6 accordance with the desired phase relationships among the plurality of clocks.

1 5. The system of claim 4, wherein the clock scheduler further comprises:  
2 toggle point logic for determining a next toggle point among the plurality of clocks; and  
3 trigger logic for generating the trigger signal for the clock associated with the next toggle  
4 point.

1 6. The system of claim 4, wherein each of the plurality of clock generation slices further  
2 comprises:  
3 toggle generation logic for toggling a logic state of the clock associated with the clock

4 generation slice in response to a toggle signal; and

5 toggle signal generation logic for generating the toggle signal if the time duration from the  
6 current time to the next toggle point among the plurality of clock generation slices is the lowest.

1 7. The system of claim 1, further comprising:

2 a target system for receiving a first data from the evaluation logic and delivering a second  
3 data to the evaluation logic, wherein the target system is controlled by the plurality of  
4 asynchronous clocks generated by the clock generation logic.

1 8. A clock generation logic system for generating a plurality of asynchronous clocks,  
2 comprising:

3 a plurality of clock generation slices for generating a plurality of clocks, where each clock  
4 generation slice generates a clock in response to a trigger signal; and

5 a clock scheduler for generating the trigger signal to the plurality of clock generation  
6 slices so that the generation of the clocks by the plurality of clock generation slices is scheduled in  
accordance with the desired phase relationships among the plurality of clocks.

1 9. The system of claim 8, wherein the clock scheduler further comprises:

2 toggle point logic for determining a next toggle point among the plurality of clocks; and  
3 trigger logic for generating the trigger signal for the clock associated with the next toggle  
4 point.

1 10. The system of claim 8, wherein each of the plurality of clock generation slices further  
2 comprises:

3 toggle generation logic for toggling a logic state of the clock associated with the clock  
4 generation slice in response to a toggle signal; and

5 toggle signal generation logic for generating the toggle signal if the time duration from the  
6 current time to the next toggle point among the plurality of clock generation slices is the lowest.

1 11. A method of verifying the proper operation of a user design, comprising steps:

2 providing a hardware model of the user design among a plurality of reconfigurable chips;  
3 generating a plurality of asynchronous clocks for driving the hardware model;

4 providing input data to the hardware model for evaluation during an evaluation period; and  
5 controlling the phase relationship among the plurality of asynchronous clocks during the  
6 evaluation period.

1 12. The method of claim 11, wherein the step of controlling further comprises steps:  
2 determining a current time;  
3 determining a next toggle point from among the plurality of asynchronous clocks from the  
4 current time; and  
5 toggling the clock associated with the next toggle point.

1 13. The method of claim 12, further comprising step:  
2 updating the current time with the time associated with this next toggle point; and  
3 determining a new next toggle point from among the plurality of asynchronous clocks  
4 from the updated current time.

1 14. The method of claim 12, wherein the step of determining the next toggle point further  
2 comprises:  
3 determining a time duration from the current time to the next toggle point for each of the  
4 plurality of asynchronous clocks; and  
5 selecting the lowest time duration from among the time durations of the plurality of  
6 asynchronous clocks.

1 15. A method of generating a plurality of asynchronous clocks, where each clock includes a  
2 plurality of toggle points and a toggle point represents a point in time where the logic state of the  
3 clock changes, comprising steps:  
4 determining a first current time;  
5 determining a first time duration from the first current time to each clock's next toggle  
6 point;  
7 comparing each clock's respective first time durations;  
8 selecting the clock associated with the lowest value among the first time durations; and  
9 toggling the logic state of the selected clock.

1 16. The method of claim 15, further comprising steps:  
2 updating the first current time with a second current time where the second current time is  
3 the time associated with this next toggle point; and  
4 determining an adjusted time duration from the updated current time to each clock's next  
5 toggle point.

1 17. The method of claim 16, wherein the step of determining the adjusted time duration  
2 includes:  
3 determining a differential time duration from the first current time to the second current  
4 time; and  
5 subtracting the differential time duration from each unselected clock's respective first time  
6 duration to generate the adjusted time duration.

1 18. The method of claim 17, further comprising steps:  
2 determining a second next toggle point for the selected clock; and  
3 determining a second time duration from the second current time to the second next toggle  
4 point.

1 19. The method of claim 18, further comprising steps:  
2 comparing the adjusted time duration of each of the nonselected clocks and the second  
3 time duration of the selected clock; and  
4 selecting the clock associated with the lowest of any of the adjusted time durations and the  
5 second time duration.

1 20. The method of claim 19, further comprising step:  
2 toggling the logic state of the selected clock.